GIGABIT 4-PHASE MODULATION-DEMODULATION CIRCUITS FOR MICROWAVE DIGITAL SYSTEMS

K. Miyauchi, S. Seki and K. Yanagimoto
Yokosuka Electrical Communication Laboratory
Nippon Telegraph and Telephone Public Corporation
1-2356 Take, Yokosuka-Shi, 238-03, Japan

ABSTRACT

An extremely high speed modulation-demodulation performance is discussed when data-rate becomes close to carrier frequency. A 4-phase PSK modulation-demodulation circuit with a newly designed transformer is described. The error-rate performance on 1.6 Gb/s data-rate was successfully undertaken at a 1.7 GHz carrier frequency.

1. Introduction

With the aid of recent advancement in various high-speed and wideband solid state microwave devices, various efforts were made to obtain gigabit microwave PSK modulation-demodulation feasibility.[1] This paper discusses high-speed microwave PSK modulator-demodulator circuits above a gigabit data-rate, putting special emphasis on the case when data-rate becomes close to carrier frequency.

Coupling economical consideration with future monolithic microwave amplifier feasibility, selection of lower carrier frequency may be desirable, especially in case of selecting an intermediate frequency in high-speed microwave or millimeter-wave communication systems. In the high-speed modulator-demodulator circuit design, separation of modulated spectrum from baseband harmonics and vice versa must be carefully taken into consideration, when the carrier frequency and the data-rate are not widely separated from each other.

2. Comparison of Various Modulator-Demodulator Circuits

Typical PSK modulators are depicted in Fig. 1. Path length modulators have been widely used hitherto, but they are not desirable, because pulse width variation occurs in accordance with the path length difference. Moreover, baseband pulse harmonics leak through the output port when pulse repetition rate is close to the carrier frequency.[2] Double balanced modulators are advantageous in this connection. The circuit (b-2) was successfully devised in ECL recently.[3] It was demonstrated that a dual-gate FET had significantly high-speed switching characteristic[4] and a PSK circuit concept was proposed,[1] but the actual PSK modulator performance is yet unknown. Table 1 shows various high-speed modulation-demodulation experiments hitherto undertaken. The error-rate performance with a data-rate above one gigabit was examined in the experiment 2 for the first time, which is discussed in detail in this paper.

3. Consideration on Highest Clock Rate with Regard to Carrier Frequency

The following impairments would cause modulation-demodulation performance deterioration, especially when extremely high data-rate would be used on a given carrier frequency;

(a) Folded component of PSK signal beyond zero frequency.
(b) Undesired harmonic components of PSK signals and/or baseband pulses leakage.
(c) Pulse width variation or jitter.
(d) Amplitude and phase errors.
(e) Slow switching response.

Impairment parameter (a) is essential, independent of modulator-demodulator circuit construction. It determines the clock frequency upper bound when carrier frequency is fixed.

The path length modulators shown in Fig. 1 (a) are not desirable for the present purpose, since impairments (b) and (c) will be dominant as mentioned above.

On the other hand, double balanced modulators do not possess impairments (b) and (c) in principle, therefore they are best suited to this purpose. In case of the modulator shown in Fig. 1 (c), baseband pulses appear at the drain of each FET. Therefore, transient baseband pulse waveform should be carefully treated for eliminating impairment (b) sufficiently.

Figure 2 shows the theoretical relationship between the highest clock frequency attainable and the carrier frequency, under the condition that (A) total impairment caused by (a), (b) and (c) is less than -40 dB, (B) the rise and fall times are not greater than 0.28T where T is the pulse width. The curve a is for an ideal double balanced modulator. Curve b is for a double balanced modulator with an insufficient balance of about 70%, considering practical microwave modulators of this type. Curve c is for path length modulators, in which relatively higher carrier frequency should be adopted to obtain sufficient modulation-demodulation performance.

The authors have tried modulation-demodulation experiments in the critical region where the clock frequency and carrier frequency ratio is arround 0.5, as marks 2 and 3 indicate in Fig. 2.

4. Revised Ring Modulator-Demodulator Circuit

Contemporary lumped ring modulators are composed of circular ring cores with helically wound thin copper wires. In this circuit configuration, sufficient balance and precise modulation angle are usually difficult to obtain in high-speed microwave modulation. The authors would like to propose a new lumped ring modulator construction, as shown in Fig. 3, in which a miniatuarized cylindrical ferrite core is used and insulated thin copper wires are not wound but are directly inserted into the core.[5][6] In this construction, one can easily obtain sufficient balance and correct modulation phase angle by precisely aligning wires in the core.

5. 1.6 Gb/s 4-Phase PSK Modulation-Demodulation Experiment

(a) Experimental circuit construction

Figure 4 shows the circuit configuration of 4-phase PSK modulation-demodulation and regeneration experiments. Two revised $0/\pi$ ring modulators mentioned above are used for composing the 4-phase modulator. A specially developed wide band 3 dB Y-junction hybrid is used to combine two $0/\pi$ PSK signals without arising undesired leaks from one modulator to the other at the combining hybrid, which causes undesired echo responses in the output 4-phase PSK signal.

At the demodulation portion, the same type of new ring modulators were used. The high-speed decision circuit[8] was used to evaluate error-rate performance at 0.8 GHz clock rate. A Thomson type band pass filter with 960 MHz bandwidth at the 3 dB attenuation point is

used to evaluate transmission characteristic.

(b) 4-Phase PSK modulation characteristic

The 4-phase PSK modulation waveforms and angle errors are measured at 1.6 Gb/s data-rate with 1.7 GHz carrier frequency. The envelope waveform is shown in Fig. 5 (a). The rise and fall times are measured as less than 250 ps. The waveform (b) in the same figure shows the dynamic responses of phase transition observed by combining the modulated signal with the continuous coherent carrier. Figure 5 (c) shows the Lissajous diagram of the 4-phase PSK signal, which indicates precise modulated phase angle, as is shown in (d). The maximum phase error was measured as less than 1.1 degree.

(c) Demodulated Eye Pattern

The demodulated eyepattern was observed as shown in Fig. 6, by inserting the Thomson type band-pass filter between modulation and demodulation portions. Eye patterns of both the in-phase channel (CH-1) and the quadrature channel (CH-2) are satisfactory, showing small interferences.

(d) Error-Rate Performance

Two independent 0.8 Gb/s pseudo-noise pulse patterns are use for measuring error-rate performance of this experimental circuit. Total band limiting characteristic is about 800 MHz or BT=1 (B: 3-dB down bandwidth), taking into account the rise and fall times of modulated signal (equivallent bandwidth of 2.7 GHz), the demodulator bandwidth characteristic (1.8 GHz) and the band pass filter bandwidth (0.96 GHz). Figure 7 shows the error-rate performance, where four different dot families correspond to 0°. 90°, 180° and 270° reference carrier phases. The reference carrier was derived from the original carrier oscillator for experimental convenience. The carrier to noise ratio (C/N) degradation from the theoretical curve (dotted line) is measured as 2.3 dB at the 10^{-9} error-rate. The degradation was relatively small, considering the relationship between data-rate and carrier frequency.

The authors extended the experiment to a case where clock frequency was 1.6 GHz and carrier frequency was 3 GHz, with the same type of ring modulator-demodulator circuit (3 in Fig. 2). The modulated waveform and the demodulated eye pattern of a two-phase PSK signal were satisfactory.(6)

6. Conclusion

It was theoretically and experimentally confirmed that a data-rate of up to a carrier frequency is attainable in the microwave 4-phase PSK modulation-demodulation It is concluded that several gigabits data-rate transmission is possible on a 1.7 to 6 GHz microwave carrier.(2)(6)

Reference

(1) C. L. Cuccia, et al,"PSK and QPSK Modulators for Gigabit Data Rates", 1977 IEEE MTT-S Int. Microw. Symp. Digest, p. 208.
(2) H. Ishio, et al, "High Speed 4-Phase PSK MODEM Circuits", Rev. of the ECL, 23, 7-8, p. 919.
(3) M. Aikawa, et al, "2 Gb/s Double-Balanced PSK Modulator Using Coplanar Waveguides", IEEE, '79 ISSCC.
(4) C. A. Liechti, "Characteristics of Dual-Gate GaAs MESFETs", 4th European Microw. Conf. p. 87, 1974
(5) S. Sato, et al, "Line Type Transformer Utilizing Ferrite Core", Trans. IECE Jap., 55-C, 10, p. 544, 1972.
(6) K. Yanagimoto, et al, "High Speed Ferrite Core Ring Modulator in Microwave Region", Trans. IECE Jap., 60-B, 2, p. 150, 1977.
(7) S. Machida, et al, "Integrated Circuits for High Speed Modulation and Demodulation", Rev. of the ECL, 23, 7-8, p. 1975.
(8) K. Kameo, et al, "800 MB High Speed Regenerator", Trans. IECE Jap., 60-B, 12, p. 984, 1977.

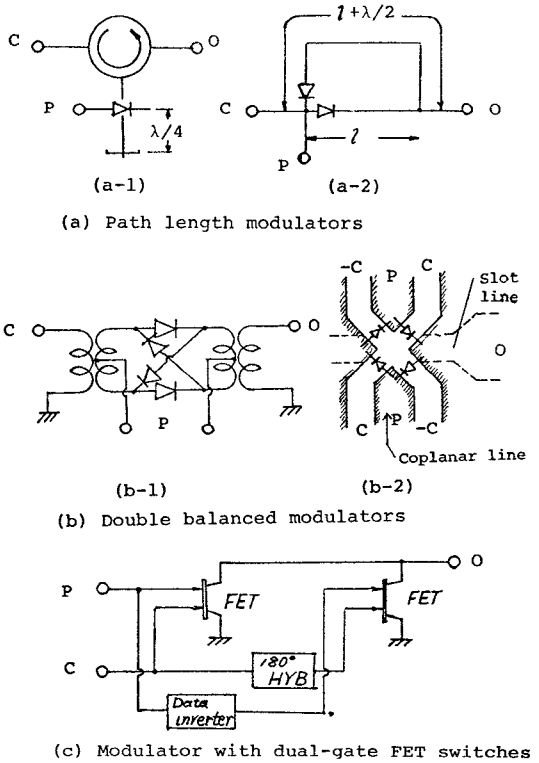


Fig. 1 Typical PSK Modulators

(C: Carrier input, O: Modulator output
P: Pulse input)

Table 1. Comparison of Various High-Speed Modulator-Demodulator Experiment Results

Modulation Format	4-phase PSK	4-phase PSK	2-phase PSK	2-phase PSK	ASK
Carrier: f_0 (GHz)	1.7	1.7	3	6	8
Bit Rate (Gb/s)	0.8	1.6	1.6	2	
Clock: f_T (GHz)	0.4	0.8	1.6	2	
f_T/f_0	0.24	0.47	0.53	0.33	*
Modulator Type	d.b.**	d.b.***	d.b.***	d.b.****	dual gate FET SW
Demodulator Type	d.b.**	d.b.***	d.b.***	—	—
Decision Circuit	Tr.HIC	Tr.HIC	—	—	—
C/N degradation at 10 (dB)	1.0	2.3	—	—	—
Organization	ECL	ECL	ECL	ECL	H.P.
Year Reported	1974	1979	1977	1979	1974

* : 70 ps rise/fall time
d.b.** : double balanced. (circular ring core)
d.b.*** : double balanced. (cylindrical core)
d.b.**** : double balanced. (coplanar waveguide)

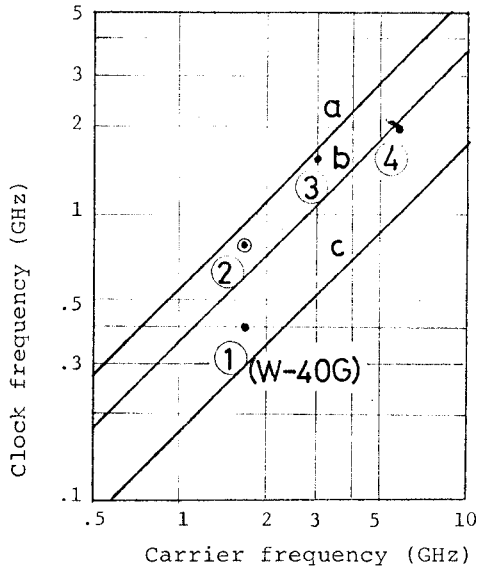
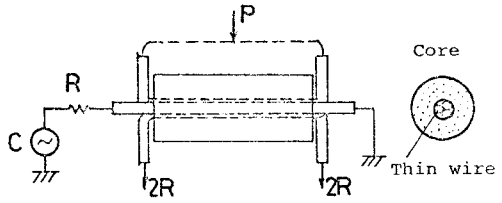
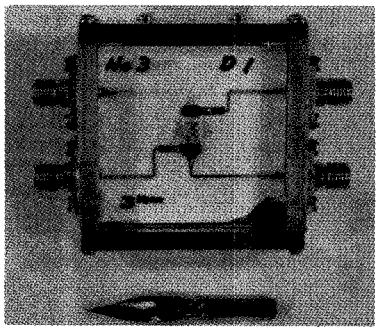


Fig. 2 Highest Attainable Clock Frequency



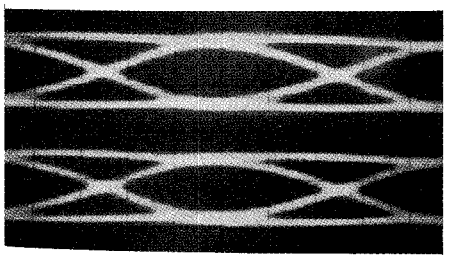
(a) Modified Transformer



(C: Carrier input, O: Modulator output, P: Pulse input)

(b) 0/π Ring Modulator

Fig. 3 1.7 GHz Modified Ring Modulator



Horizontal 250 ps/div.

Fig. 6 Demodulated Eyepattern

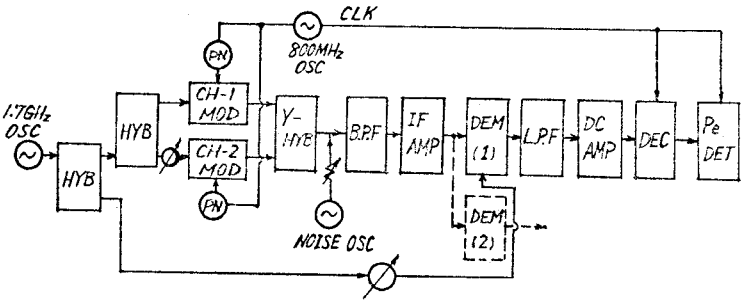
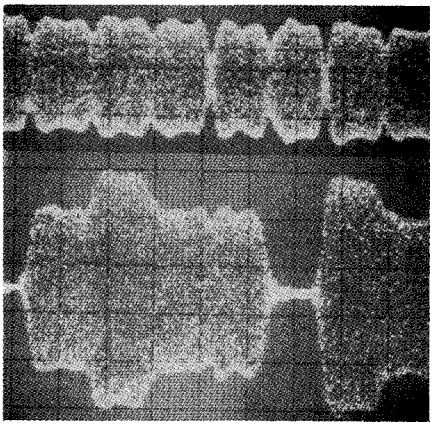


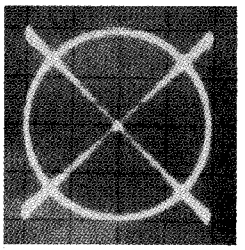
Fig. 4 Circuit Construction of 1.6 Gb/s 4-Phase PSK Error-Rate Performance Experiment

(a) Envelope Waveform

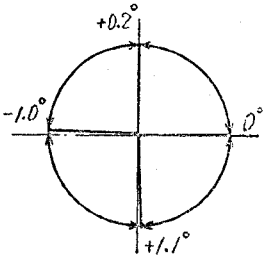
(b) Phase Waveform



Horizontal: 1 ns/div.



(c) Lissajous Diagram



(d) Phase Errors

Fig. 5 1.6 Gb/s 4-Phase PSK Modulator Performance

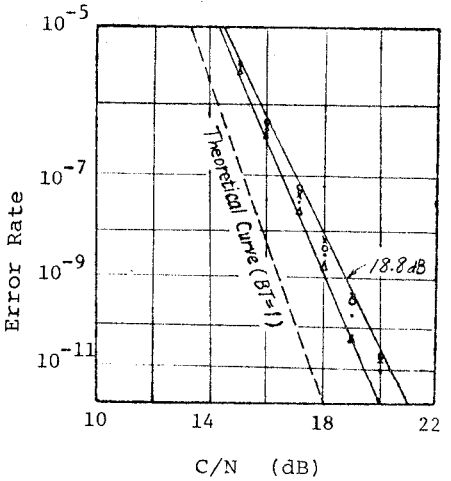


Fig. 7 1.6 Gb/s 4-Phase PSK Modulation-Demodulation Error-Rate Performance